PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/790,689
Filing Date:	March 3, 2004
Applicant:	Pierte Roo
Group Art Unit:	2611
Examiner:	Siu M. Lee
Title:	SYSTEM AND METHOD FOR REDUCING ELECTROMAGNETIC INTERFERENCE AND GROUND BOUNCE IN AN INFORMATION COMMUNICATION SYSTEM BY CONTROLLING PHASE OF CLOCK SIGNALS AMONG A PLURALITY OF INFORMATION COMMUNICATION DEVICES
Attorney Docket:	MP0304

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

DECLARATION UNDER 37 C.F.R. § 1.131

I, Pierte Roo, hereby declare as follows:

1. I am the inventor of the subject matter claimed in U.S. Application No. 10/790,689 ("the '689 application").

2. I understand that U.S. Patent No. 6,946,870 by Austin Lesea, entitled "Control of Simultaneous Switch Noise from Multiple Outputs" ("the '870 patent"), has been cited as prior art against the '689 application. That in a Non-Final Office Action dated January 22, 2008, all claims were rejected under 35 U.S.C. § 102(e) as being

anticipated by the '870 patent, or as being unpatentable over the '870 patent in combination with one or more other references.

3. The '870 patent issued from U.S. Application No. 10/691,146 ("the '146 application") filed on October 21, 2003.

4. Prior to October 21, 2003, the invention which is the subject matter of the '689 application was conceived in the United States and reduced to practice.

5. I am the author of the materials attached at Exhibit B.

6. That the invention was conceived prior to October 21, 2003, as evidenced by Exhibits A and B.

7. That the materials attached at Exhibits A and B have dates that are blacked out which pre-date October 21, 2003.

8. That the invention has never been abandoned, suppressed, or concealed.

9. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are being made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false

statements may jeopardize the validity of the application, and patent issuing thereon, or any patent to which this verified statement is directed.

Dated: 7/17/2008

Pierre Roo

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EXHIBIT A

[redacted]

Via Facsimile (202) 298-7570
Confirmation Via Federal Express
Richard P. Bauer, Esq.
Katten Muchin Zavis
1025 Thomas Jefferson St., NW
Washington, DC 20007-5201

Re: New U.S. Patent Application: Gigabit Transmit Clocking for Reducing EMI and Supply Bounce
Our Docket No.: MP0304
Your Reference No.:
Requirements: Prepare new patent application
Marvell Target Date: November 14, 2003

Dear Rick:

We would like you to prepare a patent application directed to the above-identified invention by no later than November 14, 2003. Please find enclosed documents describing the invention along with a videotape of an invention disclosure interview.

The inventorship information is as follows:

Inventor	Citizenship	Address	City	State	Zip	Country
Roo, Pierte	US	144 Holly Ct.	Mountain View	CA	94043	US

Please review the enclosed materials and before proceeding please provide your estimate as to cost and schedule.

Please also prepare a declaration and assignments as follows.

X Inventor to Marvell Semiconductor Inc.

X Marvell Semiconductor Inc. to Marvell International, Ltd.

The final deliverables will include an electronic version **and a claim tree.**

Please do not hesitate to contact me if you have any questions.

With warmest regards.

Very truly yours,

Amanda J. Gray on behalf:

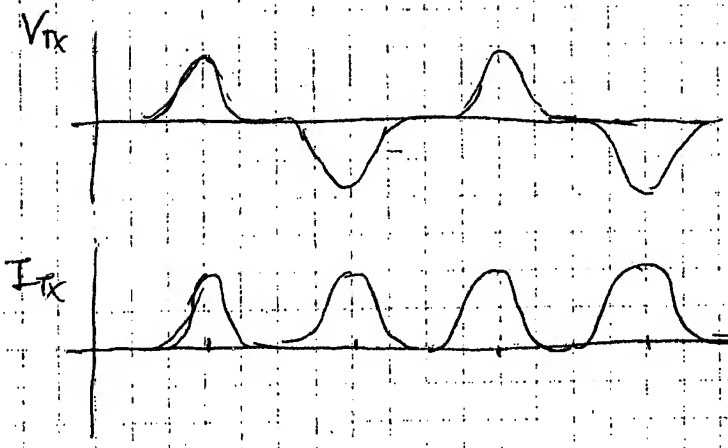
Eric Janofsky
General Patent Counsel

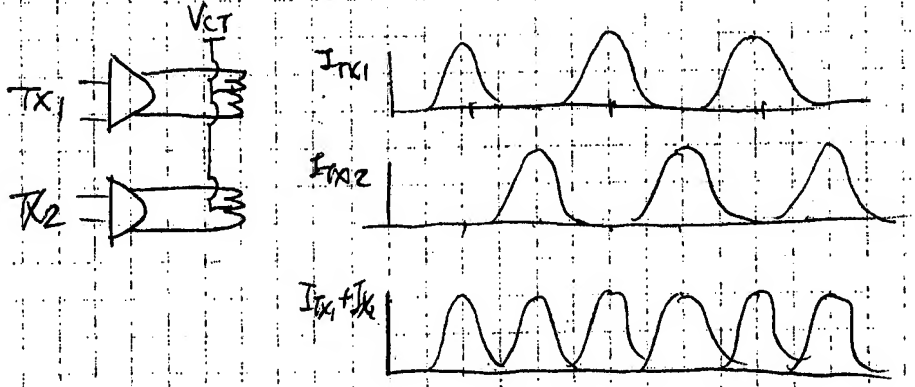
EBJ:ajg
Enclosures: Invention documents (Confirmation Copy)
Video Tape (Confirmation Copy)

EXHIBIT B

[redacted]

EMI

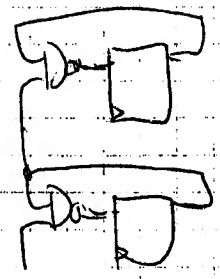


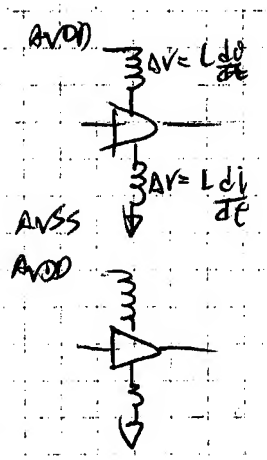


Mixing clock phase

- ✓ local — pair to pair — adjacent pairs.
- ✓ global — port to port — Multi ports.
  adjacent phy.

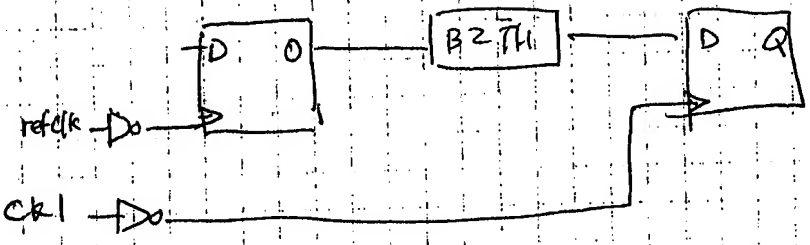
- reduce EMI
- reduce requirement for common-mode choke

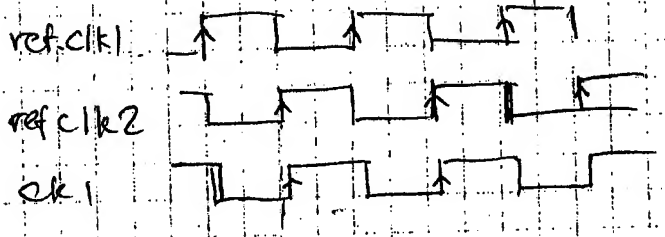




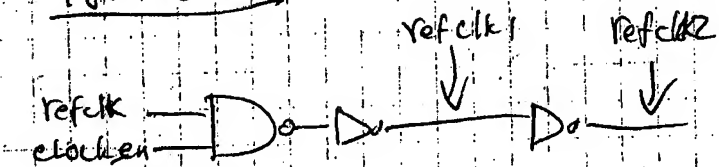
Improvement → - Reduce Power supply bounce
- Reduce EMI. (clock switch a different time).

Decoder



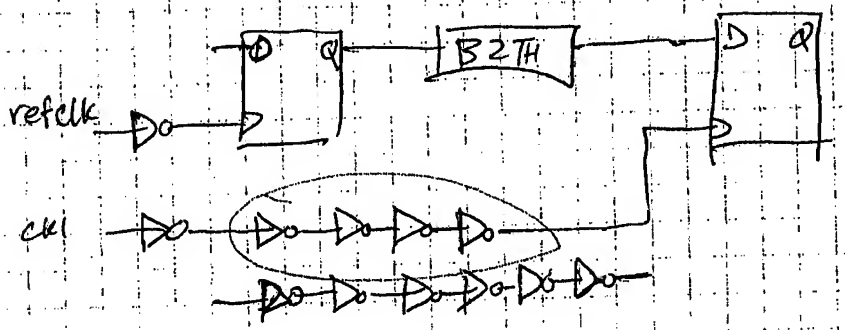


- refclk 2 (inverted from refclk1) is the input to DLL giving 180° shift.

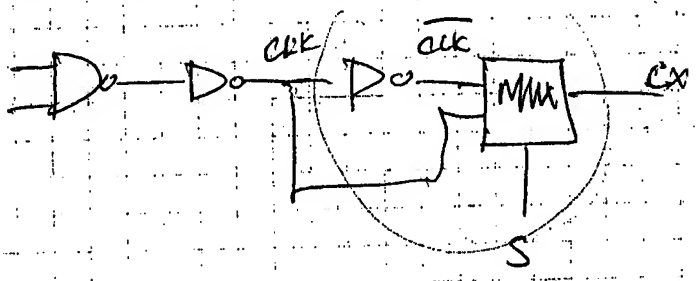


Changes

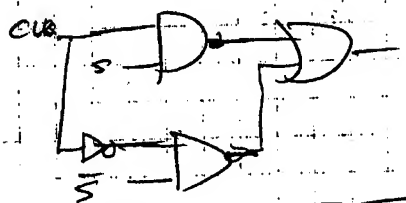
① change decoder to have clock delay



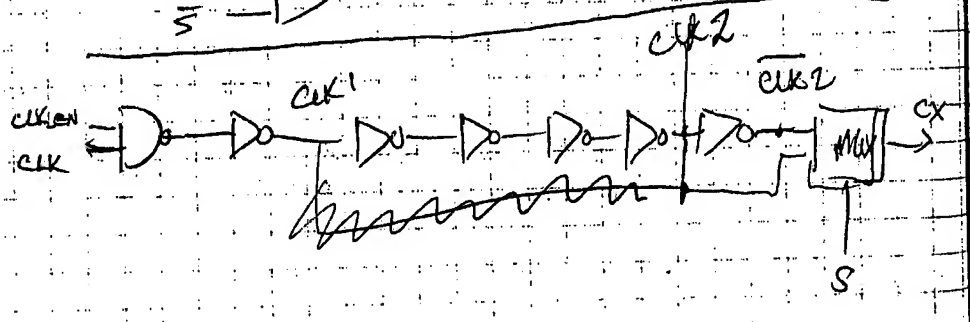
(2) refclk inversion - selectable



$$CX = CLK\,S + \overline{CLK}\,\overline{S}$$



(?)



[redacted]

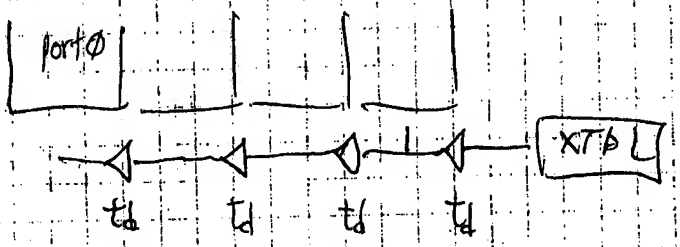
TXDAC phisel

ch0	ch1	ch2	ch3
0	180	0	180

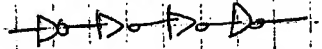
Reg 30_33:15:12 = 1010 (3210)

TBG init

4 ports

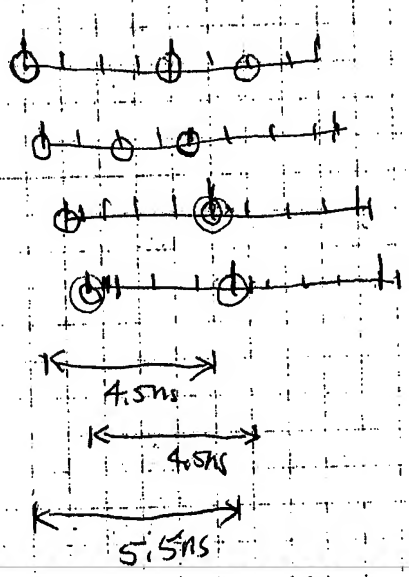


td = 4 inverts



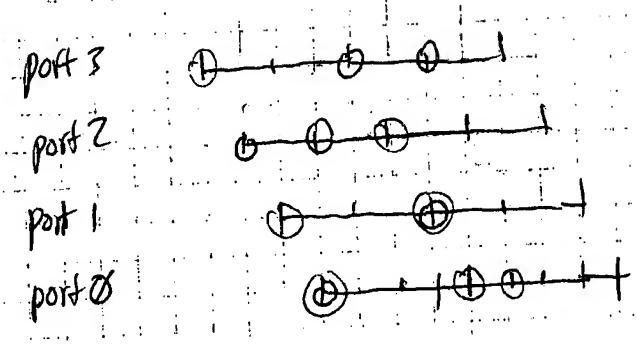
td = varies from 0.4ns → 1.0ns

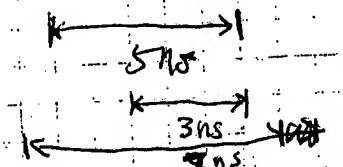
td = 0.4ns



	180	270°	0
	0°	90°	180
	180°	180°	90
	0°	0°	180

$t_d = 1\,ns$

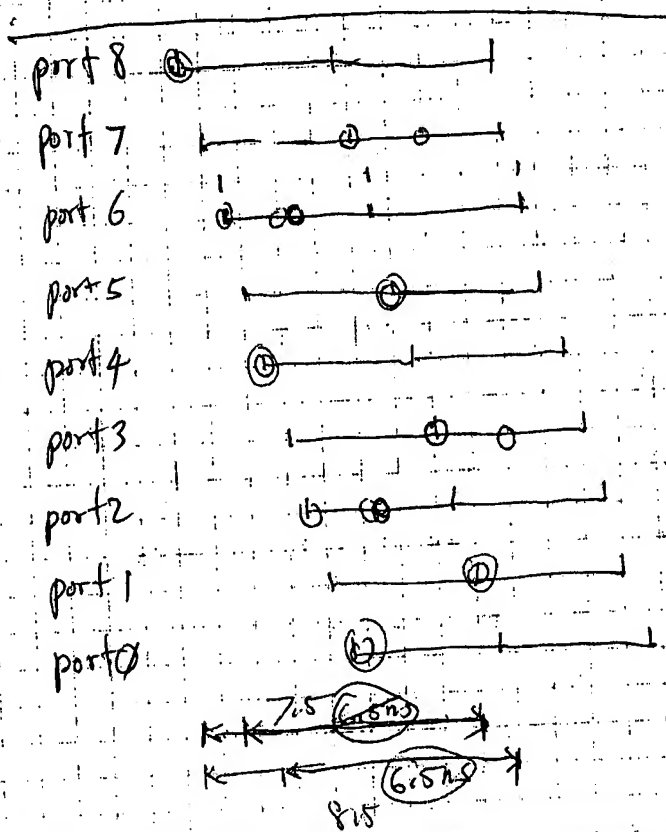




best choice is 180°, 0°, 180°, 0° (3210)

9 ports

$t_d = 0.5\,ns$



8.5